REMARKS

The claims are claims 1 to 4.

Claims 11 to 14 are newly canceled

Claims 1 to 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Frankel et al U.S. Patent 4,463,443 and Steinmetz et al U.S. Patent 5,809,521.

Claims 1 recites subject matter not made obvious by the combination of Frankel et al and Steinmetz et al. Claim 1 recites a copy/access controller "operable to copy data from said first buffer to said second buffer when said first buffer is substantially full" and "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." These limitations are not made obvious by the combination of Frankel et al and Steinmetz et al. The FINAL REJECTION states at page 2, line 23 to page 3, line 1:

> "Frankel fails to explicitly teach the prompting of a second component to access the second buffer when the data is copied from the first buffer. However, it was notoriously well known in the art at the time of invention to use signal to prompt buffer connected devices to read and write data to and from the buffer."

The Applicants submit that the above quoted language of claim 1 requires more than merely writing to the output shift register. This language requires generation of a prompt signal to initiate reading data by the second component. The Applicants submit this limitation is not inherent in the mere writing of data to the buffer. The FINAL REJECTION cites element 16 and nEMPTY signal illustrated in Figure 1b and column 3, line 40 to column 4, line 5 of the secondary reference Steinmetz et al as making obvious this subject matter. Steinmetz et al states at column 3, line 62 to column 4, line 1 (within the section cited by the Examiner):

> "Each FIFO memory is cascaded by connecting the "not empty" (nEMPTY) signal of one FIFO to the write terminal of the succeeding FIFO, the "not full" (nFULL) signal to the read terminal of the preceding FIFO and the data output terminal (DATAOUT) of one FIFO to the data input (DATAIN) terminal of the succeeding FIFO."

The Applicant assumes that the Examiner's position is that the nEMPTY signal of FIFO 16 causes the not illustrated receiving system to read data out of FIFO 16. This teaching of Steinmetz et al differs from the above quoted language of claim 1 because there is not a single structure (the claimed copy/access controller) which both copies data to the second buffer and prompts the second component to access the second buffer. This subject matter is illustrated at element 24 in Figure 4 of this application. In particular, there is no disclosure in Steinmetz et al that the nEMPTY signal of FIFO is generated by the same component that copies data into the second buffer. Accordingly, claim 1 is allowable over the combination of Frankel et al and Steinmetz et al.

Claims 2 to 4 are allowable by dependence upon respective allowable base claim 1.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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